

## EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L5	3868	(716/2,3,8,11.ccls. or 703/1.ccls.)	US-PGPUB; USPAT	OR	ON	2006/07/15 09:05
L8	673	((widest or largest or biggest) near5 transistor)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/07/15 09:07
L10	4078	((fold\$4 or compact\$4) near10 transistor)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/07/15 09:23
L12	32	8 and 10	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/07/15 09:12
L13	5	5 and 12	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/07/15 09:22
L14	129	(height adj2 bound)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/07/15 09:22
L15	1	10 and 14	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/07/15 09:23
L16	1	8 and 14	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/07/15 09:23
L17	5	((fold\$4 or compact\$4) near10 transistor) same (U adj shape or U-shape or finger or leg) same (equal or equivalent)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/07/15 09:24

## EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L2	1	716/2,3,8,11.ccls. and ((fold\$4 near10 (widest or biggest or largest) near5 transistor) and (width near10 (height adj3 bound))).clm.	US-PGPUB; USPAT	OR	ON	2006/07/15 09:01
L3	1	716/2,3,8,11.ccls. and ((fold\$4 near10 (widest or biggest or largest) near5 transistor) and (width near10 ((height adj3 bound) or predetermin\$3 or threshold))).clm.	US-PGPUB; USPAT	OR	ON	2006/07/15 09:02
L4	1	((fold\$4 near10 (widest or biggest or largest) near5 transistor) and (width near10 ((height adj3 bound) or predetermin\$3 or threshold))).clm.	US-PGPUB; USPAT	OR	ON	2006/07/15 09:02



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» Key

IEEE JNL IEEE Journal or Magazine

IEE JNL IEE Journal or Magazine

IEEE CNF IEEE Conference Proceeding

IEE CNF IEE Conference Proceeding

IEEE STD IEEE Standard

#### 1. Design techniques for a 1-V operation Bluetooth RF transceiver

Ugajin, M.; Yamagishi, A.; Kodate, J.; Harada, M.; Tsukahara, T.;  
[Custom Integrated Circuits Conference, 2004. Proceedings of the IEEE 2004](#)  
 3-6 Oct. 2004 Page(s):393 - 400

[AbstractPlus](#) | Full Text: [PDF\(740 KB\)](#) IEEE CNF  
[Rights and Permissions](#)

#### 2. Optimal 2-D cell layout with integrated transistor folding

Gupta, A.; Hayes, J.P.;  
[Computer-Aided Design, 1998. ICCAD 98. Digest of Technical Papers, 1998 IEEE/ACM International Conference on](#)  
 8-12 Nov 1998 Page(s):128 - 135

[AbstractPlus](#) | Full Text: [PDF\(840 KB\)](#) IEEE CNF  
[Rights and Permissions](#)

#### 3. Doubly folded transistor matrix layout

van Gennepen, L.P.P.P.; van Eijndhoven, J.T.J.; Brouwers, J.A.H.C.M.;  
[Computer-Aided Design, 1988. ICCAD-88. Digest of Technical Papers, IEEE International Conference on](#)  
 7-10 Nov. 1988 Page(s):134 - 137

Digital Object Identifier 10.1109/ICCAD.1988.122479  
[AbstractPlus](#) | Full Text: [PDF\(368 KB\)](#) IEEE CNF  
[Rights and Permissions](#)

#### 4. A multiple-row transistor placement system for full custom design

Yih-Chih Chou; Jian-Hung Chen; Yang, M.; Shyh-Chang Lin;  
[VLSI Design, Automation and Test, 2005. \(VLSI-TSA-DAT\). 2005 IEEE VLSI-TSA International Symposium on](#)  
 27-29 April 2005 Page(s):136 - 139

[AbstractPlus](#) | Full Text: [PDF\(252 KB\)](#) IEEE CNF  
[Rights and Permissions](#)

#### 5. A transistor sizing method applied to an automatic layout generation tool

Santos, C.; Wilke, G.; Lazzari, C.; Reis, R.; Guntzel, J.L.;  
[Integrated Circuits and Systems Design, 2003. SBCCI 2003. Proceedings. 16th Symposium on](#)  
 8-11 Sept. 2003 Page(s):303 - 307

[AbstractPlus](#) | Full Text: [PDF\(256 KB\)](#) IEEE CNF  
[Rights and Permissions](#)

6. Design of CMOS composite transistors with improved operating region  
Young-Gyu Yu; Seok-Woo Choi; Dong-Yong Kim; Kyu-Tae Park; Hong-Jo Ahn;  
Circuits and Systems, 2000. Proceedings of the 43rd IEEE Midwest Symposium on  
Volume 3, 8-11 Aug. 2000 Page(s):1034 - 1037 vol.3  
Digital Object Identifier 10.1109/MWSCAS.2000.951393  
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